Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("5675684").PN.	USPAT	OR	OFF	2004/12/09 14:12
L2	1	("5196371").PN.	USPAT	OR	OFF	2004/12/09 14:00
L3	1	("20030102566").PN.	US-PGPUB; USPAT	OR	OFF	2004/12/09 14:15
L4	1	("6524346").PN.	US-PGPUB; USPAT	OR	OFF	2004/12/09 14:28
L5	6	((chip or die) with (sink or spreader)) and (laser with (encapsulation or encapsulating))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:05
L6	1	L1 and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:50
L7	24	((chip or die) with (sink or spreader)) and (laser with (encapsulant or encapsulation or encapsulating))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:22
L8	14	L7 and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 14:52
L9	5	"6544814"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 14:42
L10	455	(@ad<"20000816") and (laser with (encapsulate or encapsulant or encapsulation or encapsulating))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:05
L11	448	L10 not (laser near (cure or cured or curing))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:24

L12	183	L11 and (chip or die or chips or dies)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:47
L13	3	("6379988").URPN.	USPAT	OR	OFF	2004/12/09 15:06
L14	8	("5471087" | "5773323" | "5855727" | "5863810" | "5897338" | "5932061" | "6069392" | "6136212").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/09 15:06
L15	167	(decapsulation or decapsulating) and (chip or die or chips or dies)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:41
L16	91	L15 and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:07
L17	91	L16 and (chip or die or chips or dies)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:47
L18	44	L17 and (wire or wires)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:53
L19	11	L16 and laser	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:48
L20	907	(chip or die) and (laser with (epoxy or encapsulation or encapsulating))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:50

L21	460	L20 and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:50
L22	241	L21 and (wire or wires)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:53
L23	237	L22 not (laser near (cure or cured or curing))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 15:54
L24	162	L23 not (laser near diode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:28
L25	0	438/940.ccls. and ((chip or die) with (sink or spreader)) and (encapsulation or encapsulating or epoxy or encapsulate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:07
L26	28	438/940.ccls. and (encapsulation or encapsulating or epoxy or encapsulate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:07
L27	26	L26 and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:11
L28	1	("6544814").PN.	USPAT	OR	OFF	2004/12/09 16:19
L29	6	(("5344795") or ("5371404") or ("5394010") or ("6218731") or ("6667544") or ("6774473")).PN.	USPAT	OR	OFF	2004/12/09 16:21
L30	0	L29 and laser	USPAT	OR	OFF	2004/12/09 16:21
L31	6	L29 and chip	USPAT	OR	OFF	2004/12/09 16:21

L32	0	438/663.ccls. and (laser with (encapsulant or encapsulation or encapsulating)) and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:23
L33	0	438/662.ccls. and (laser with (encapsulant or encapsulation or encapsulating)) and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:23
L34	48	"438"/$.ccls. and (laser with (encapsulant or encapsulation or encapsulating)) and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:23
L35	100	"438"/$.ccls. and (laser with (epoxy or encapsulate or epoxy or encapsulant or encapsulation or encapsulating)) and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:24
L36	98	L35 not (laser near (cure or cured or curing))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:26
L37	250	"257"/$.ccls. and (laser with (epoxy or encapsulate or epoxy or encapsulant or encapsulation or encapsulating)) and (@ad<"20000816")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:26
L38	73	L37 and L36	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:26
L39	275	L37 or L36	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:26

L40	269	L39 not (laser near (cure or cured or curing))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:26
L41	213	L40 not (laser near diode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/09 16:28

Capte et al

portion 39 is applied in liquid form to either the chip 10 or the substrate 20, as shown in FIGS. 18 and 17, respectively. However, in either case, the second portion most preferably remains liquid during the reflow operation. Alternately, the second portion 39 may be applied as a solid or viscous liquid that melts to a low viscosity liquid during reflow operation to either the chip or substrate as shown in FIGS. 18 and 17, respectively.

(16) Finally, chip 10 is then positioned so that the solder bumps 14 face the substrate 20 and aligned with the solder pads 12 of the substrate. In both embodiments, the solder bumps 14 protrude beyond the first portion encapsulant 37 after the encapsulant coating step. The chip assembly 10 with its solder bumps 14 and encapsulant are moved into intimate contact with the substrate 20 and solder pads 12, respectively, such that the second portion encapsulant 39 lies between the two parts. The assembly is heated to harden the encapsulant 39 and simultaneously reflow the solder 14 using convection reflow technology, preferably in a nitrogen blanket, to attach the solder joints that form to the contact pads 12 of the substrate 20. Other heating and reflow and curing techniques, known to those skilled in the art, are possible. The encapsulant 37 and 39 provides a continuous seal between the chip 10 and the substrate 20.

(17) FIGS. 19-21 illustrate a method for creating the solder bumps where the first portion of the encapsulant 37 is solid and the first portion is applied to the chip 10 prior to the solder bumps 30 being applied. Openings 38 are created in the solid first portion 37 that expose underlying chip metallization pads 24. These openings 38 can be created by printing the first portion 37 with the openings 38 in place or by subsequently imaging and developing the first portion encapsulant or drilling the first portion 37 with lasers, plasmas, or chemical enchants or other means know in the art. Alternatively, if the first portion is applied in a laminated tape form, the openings may be drilled or punched in the tape prior to application to the chip. This would require that the openings in the tape be

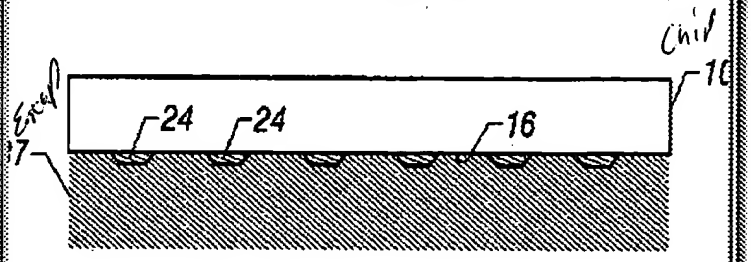

FIG. 19

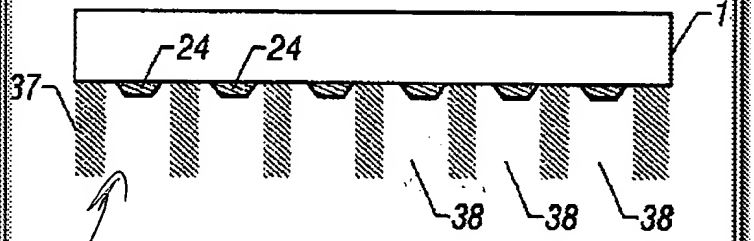

FIG. 20

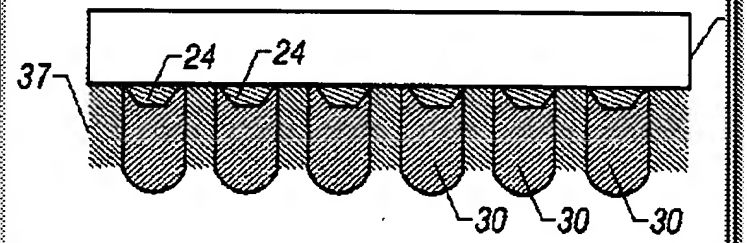

FIG. 21

102 7-94 Col 10 58-60

103

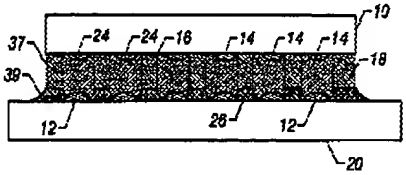

FIG. 16

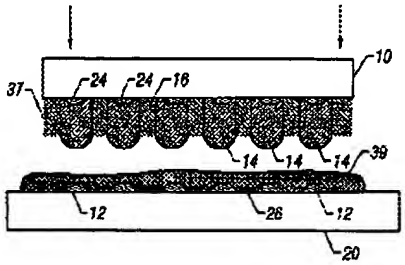

FIG. 17

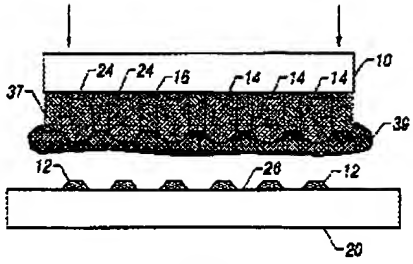

FIG. 18

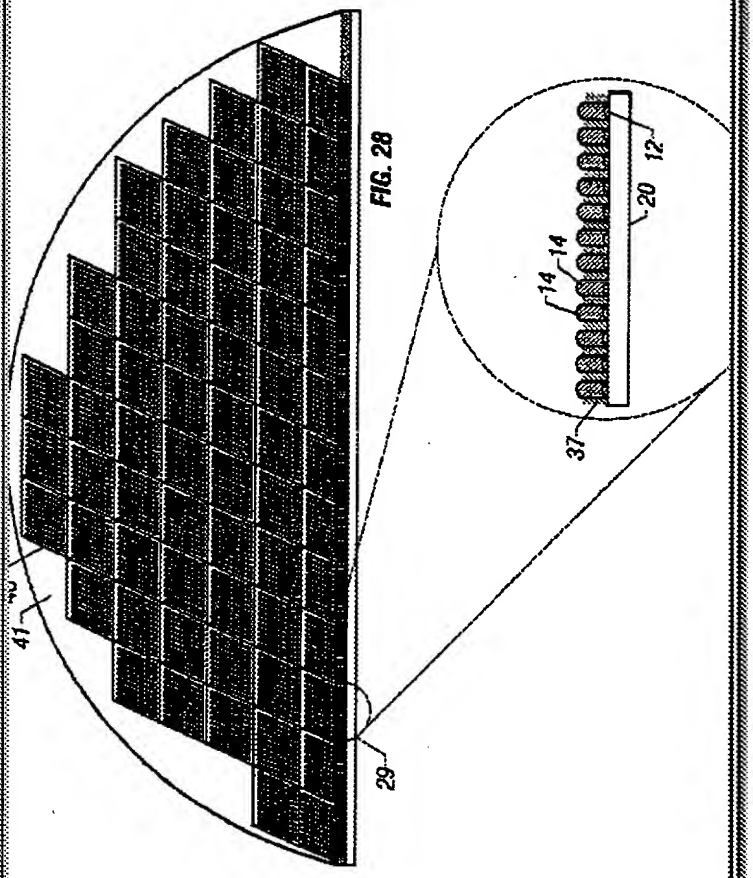

FIG. 28

US005723900A

United States Patent [19]
Kojima et al.

[11] Patent Number: 5,723,900
[45] Date of Patent: Mar. 3, 1998

[54] RESIN MOLD TYPE SEMICONDUCTOR DEVICE

[75] Inventors: Akira Kojima; Haruhiko Makino; Eiji Ohsawa, all of Kanagawa, Japan

[73] Assignee: Sony Corporation, Tokyo, Japan

[21] Appl. No.: 799,497

[22] Filed: Feb. 12, 1997

Related U.S. Application Data

[63] Continuation of Ser. No. 295,595, Sep. 2, 1994, abandoned.

[30] Foreign Application Priority Data

Sep. 6, 1993 [JP] Japan 5-221414

[51] Int. Cl.[6] H01L 23/498

[52] U.S. Cl. 257/666; 257/686; 257/692; 257/787

[58] Field of Search 257/787, 666, 257/582, 684, 705, 784, 692, 691

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Primary Examiner—Tom Thomas
Assistant Examiner—Roy Potter
Attorney, Agent, or Firm—Hill, Steadman & Simpson

[57] ABSTRACT

A thin thin resin mold semiconductor device can be provided. A resin mold type semiconductor device is arranged so that a semiconductor chip is disposed within a range of the thickness of a lead frame and sealed with a resin mold, that the thickness of the semiconductor device is defined by the thickness of the lead frame, and that an upper surface, a lower surface and a side surface of a terminal portion formed by the lead frame are exposed from the surface of the resin mold.

16 Claims, 8 Drawing Sheets

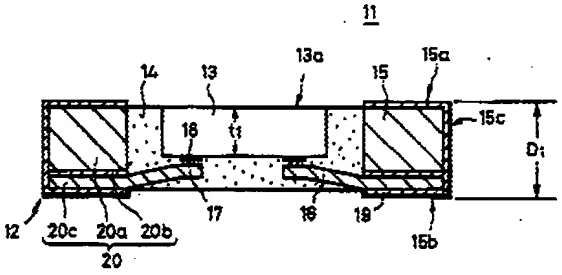

FIG. 4H

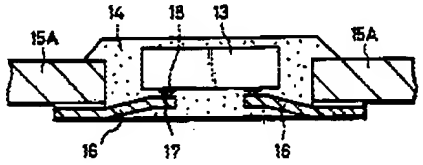

FIG. 4I

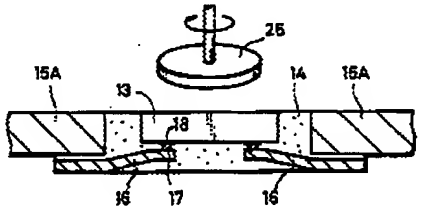

FIG. 4J